Intel® 31244 PCI-X to Serial ATA Controller

Specification Update

January 2005

Notice: The Intel® 31244 PCI-X to Serial ATA Controller may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 273794-007

Contents

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Revision History

Date	Version	Description
January 2005	007	• Added Documentation Changes 7, 8, and 9. Serial ATA *1.0**e*** should be replaced with Serial ATA *1.0**a*** in several of our documents. • Clarification on the Errata 6 that this is not an issue with the PIO Setup used in the IDENTIFY DEVICE command that uses the PIO Setup during drive initialization.
December 2004	006	• Added Errata **6** "HOLD Issue with Certain Drives" on page 13 • Added a note to Errata 3 while also indicating errata #6 supercedes this errata. Removed the workaround for Errata 3. • Added Specification Updates: - "PIO mode is no longer supported." on page 16 - "BIST mode is not longer supported." on page 16 - "Serial ATA II Native Command Queuing references should be removed." on page 17 • Added Documentation Updates: - "VCC5REF incorrectly referenced in documentation" on page 17 - "Serial ATA II Native Command Queuing references should be removed." on page 17 - "Reference to support ATAPI CD-ROM and DVD devices should be removed." on page 17 - "PIO mode references should be removed." on page 17 - "BIST mode references should be removed." on page 18
February 2004	005	• Added Errata **4** ("Non-Cache-Aligned DMA Transfers" on page 13). • Added Errata **5** ("No Reception of Spread Spectrum Clocking (SSC) Encoded Data" on page 13). • Miscellaneous edits throughout.
December 2003	004	Initial public release of this document.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® 31244 PCI-X to Serial ATA Controller Developer's Manual	273603
Intel® 31244 PCI-X to Serial ATA Controller Datasheet	273595
Intel® 31244 PCI-X to Serial ATA Controller Design Guide	273651

Nomenclature

Errata are design defects or errors. These may cause the Intel® 31244 PCI-X to Serial ATA Controller's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® 31244 PCI-X to Serial ATA Controller product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.
Plan Fix:	This erratum may be fixed in a future stepping of the product.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings	Page	Status	Errata
	C-0			
1	X	11	No Fix	Soft/Warm Boot in Master/Slave Mode
2	X	11	No Fix	Disparity Errors and Device Hanging at Boot-up
3	X	12	No Fix	**NCQ Race Conditions**
4	X	13	No Fix	**Non-Cache-Aligned DMA Transfers**
5	X	13	No Fix	**No Reception of Spread Spectrum Clocking (SSC) Encoded Data**
6	X	13	No Fix	**HOLD Issue with Certain Drives.**

Specification Changes

No.	Steppings	Page	Status	Specification Changes
	C-0			
1	X	17	No Fix	PIO mode is no longer supported.
2	X	17	No Fix	BIST mode is not longer supported.
3	X	16	No Fix	NCQ is not supported.

Specification Clarifications

No.	Steppings	Page	Status	Specification Clarifications
	C-0			

Documentation Changes

No.	Document Revision	Page	Status	Documentation Changes
1	273595-005	17	Doc	VCC5REF incorrectly referenced in documentation
2	273651-003	17	Doc	VCC5REF incorrectly referenced in documentation
3	273603-006	17	Doc	**Serial ATA II Native Command Queuing references should be removed.**
4	273603-006	17	Doc	Reference to support ATAPI CD-ROM and DVD devices should be removed.

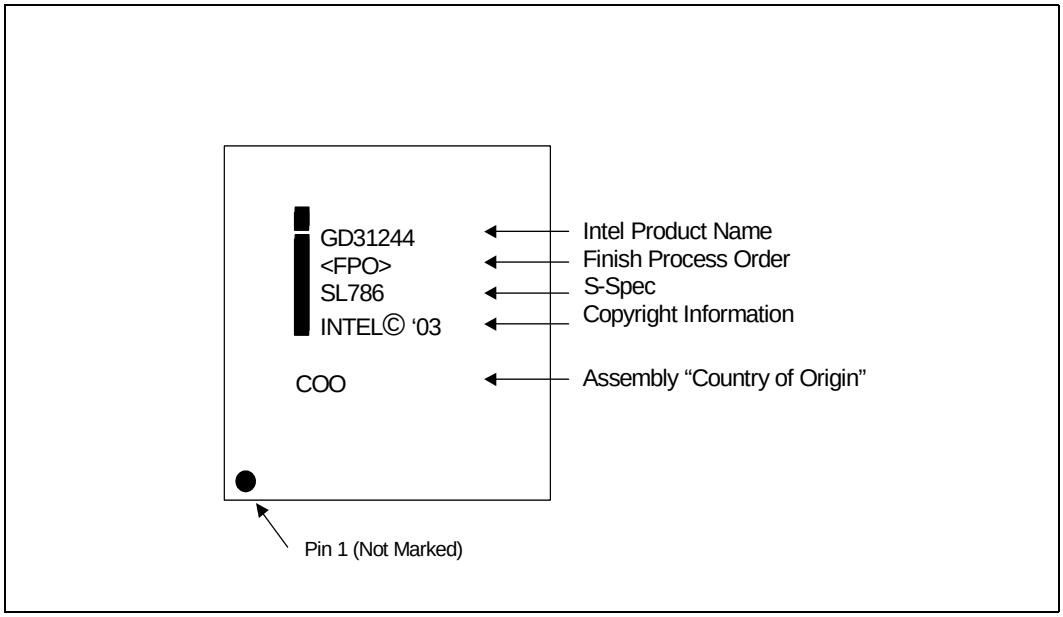
Documentation Changes

No.	Document Revision	Page	Status	Documentation Changes
5	273603-006	17	Doc	PIO mode references should be removed.
6	273603-006	18	Doc	BIST mode references should be removed.
7	273603-006	18	Doc	Incorrect reference to the Serial ATA Specification in the Design Guide
8	273595-005	18	Doc	Incorrect reference to the Serial ATA Specification in the Data Sheet
9	273651-003	19	Doc	Incorrect reference to the Serial ATA Specification in the Data Sheet

Identification Information

Markings

Figure 1. Marking Information



Stepping	Tracking Code	Notes
C0	SL786	

Errata

1. Soft/Warm Boot in Master/Slave Mode

Problem: During a soft or warm boot, the Intel® 31244 PCI-X to Serial ATA Controller (hereafter "31244") hangs when it is in Master/Slave mode.

Implication: To correctly boot the 31244 in master/slave mode, use the specific sequence detailed in the workaround section.

Workaround: **Software workaround:** Requires a driver or expansion ROM workaround. To fix the problem following a warm boot, write the Serial Control register as shown below:

1. Clear serial control register address (008h) with 0000_0000
2. Write serial control register address (008h) with 0000_0001

For bootable master/slave and DPA modes, a boot ROM must write the serial control register, as shown above, before attempting the "identify drive" command.

In a non-bootable DPA environment, the DPA driver must issue the write before enabling each SATA port (spinning up the attached drives). Note that because the register is edge-triggered it must be cleared and then set.

Status: No Fix

2. Disparity Errors and Device Hanging at Boot-up

Problem: The driver may hang intermittently as it attempts to load during boot.

Implication: Symptoms can include the following:

- Driver may not successfully load.
- OS may hang during boot.

Workaround: Add extra bulk capacitance on the printed circuit board. The following is suggested:

- An additional three 47 µF capacitors on the 3.3-volt line.
- An additional three 47 µF capacitors on the 2.5-volt line.

Status: No Fix. Follow the workaround instructions.

Note: With certain Serial ATA analyzers, this error may be more prevalent because some analyzers are susceptible to A/C voltage surges.

3. NCQ Race Conditions

Problem: With the implementation of Native Command Queuing (NCQ), a race condition occurs between the updating of the Set Device Bits (SDB) Frame Information Structure (FIS) and a PCI/PCI-X Write of the Set Device Bits FIS register.

Implication: The 31244 uses the SDB FIS to notify the host of the completion of queued commands. Within the queuing specification for Serial ATA, a race condition exists that has not been addressed by the specification or within the design of the 31244 processor.

The race condition occurs when the host software (device driver) writes the SDB word to set the queued command's busy bit, simultaneously with the receipt of an SDB FIS (one clock after the CRC is checked, the 31244 updates the SDB word with the FIS contents). The 31244 logic that implements this register contains an if–else priority encoder for the host and device update operations, with the PCI-X write being the higher priority. During an occurrence of the race condition, the update of the data for the SDB word from the device FIS is lost. The result is that commands time-out, waiting for a completion status that would have retired these commands by the received SDB FIS.

To date there is no indication that this event has occurred in a normal operating system environment, but this time-out has occurred while running diagnostic software.

Note: This error is not a data-integrity issue. All data transfers to/from the disk are completed. Only the completion status of those commands is lost. This results in the host driver timing out the commands associated with the SDB FIS that were lost. A retry of those commands does complete normally.

Workaround: Refer to erratum #6

Status: No Fix. Do not enable NCQ. Refer to erratum #6

4. Non-Cache-Aligned DMA Transfers

Problem: Most operating systems program the 31244 descriptor tables for cacheline-aligned DMA transfers. However, in some cases, such as diagnostics, software might utilize descriptors that generate non-cacheline-aligned DMA transfers, which can result in data corruption.

Implication: In the 31244, the PCI-X core generates invalid byte-enables when the DMA engine makes a multiple cacheline-sized, non-aligned MWI transfer request to the core, which is supposed to demote the transfer to a Memory Write. When the PCI bus GNT# signal is asserted in one particular clock time relative to FRAME# assertion, the core demotes the command type but not the byte enables, resulting in data corruption.

Workaround: The software workaround is to configure the DMA engine to prevent it from making non-aligned MWI requests. You can do this using one of two methods:

- **Either** enable “cacheline alignment” in the DMA engine's transfer request logic.
- **Or** disable “block” commands.

To enable DMA engine cacheline alignment, the host must set the following registers:

- Cacheline Size Congfiguration Register 'h0C[7:0] = 'h08 | 'h10 | 'h20 | 'h40 | 'h80
- DMA Control Configuration Register 'hA0[1:0] = 2'b11 (reset values)

These values must be set as part of the initialization of the 31244 since the reset value for the cacheline size is 'h00. This is not an acceptable value because it disables cacheline alignment in the DMA engine.

Alternatively, to disable block commands the host must set DMA Control Configuration Register 'hA0[2] = 1'b1. The DMA engine then uses only Memory Read and Memory Write commands for both PCI and PCI-X transfers. This may not be a practical solution because the software does not know the difference between PCI and PCI-X and it is not normally acceptable to disable PCI-X block commands.

The MWI Enable bit in the Configuration Control Register 'h04[4] does not fix the problem. It functions to specification and is one input to the demotion logic. However, it does not fix the problem.

Status: No Fix

5. No Reception of Spread Spectrum Clocking (SSC) Encoded Data

Problem: The 31244 generates Spread Spectrum Clocking (SSC) encoded data. However, it does not receive SSC-encoded data.

Implication: The Serial ATA specification[1] states that generating SSC data is optional. However, all Serial ATA devices must be able to receive SSC data.

Workaround: To prevent problems communicating with SSC-encoded hard drives, disable this optional SSC capability and revert to non-spread-spectrum transmission mode.

Status: No Fix

6. HOLD Issue with Certain Drives

Problem: The primitive sequence of HOLD/HOLD/ALIGN/ALIGN sent by the drive during a non-DATA FIS including: Register, PIO Setup, Set Device Bits, DMA Setup and BIST Activate, can corrupt the GD31244’s internal copy of FIS (shadow taskfile registers) resulting in delays and a possible

1. Serial ATA (SATA) specification, revision 1.0a

hang condition. The internal copy of the first DWord in the FIS is correct, but the remaining data is offset by one DWord past its designated position.

Note: This is not an issue with the PIO Setup used in the IDENTIFY DEVICE command that uses the PIO Setup during drive initialization.

Implication: The non-DATA FISes with this HOLD/HOLD/ALIGN/ALIGN primitive sequence and NCQ operations, PIO data transfers, BIST are unreliable and may result in data corruption. The details are listed below in the Status section.

Workaround: Do not enable NCQ, use DMA transfers (instead of PIO) and do not use BIST.

Status: No Fix. See individual FIS commands listed below for additional details.

a. PIO Setup FIS - lock up issue

Problem: If a drive inserts an HOLD/HOLD/Align/Align sequence in a PIO Setup command FIS with GD31244 during a PIO data transfer, a hang condition can occur.

Implication: This sequence may corrupt LBA sector count, ending status and transfer count fields in the GD31244 shadow taskfile registers. Because of these fields being corrupted, PIO data transfer in DPA mode is not recommended. Note this is not a problem with IDENTIFY DEVICE command that uses the PIO Setup during drive initialization.

Workaround: Use DMA controller to do data transfers. This is a more efficient mode of transfer to optimize data throughput.

Status: No Fix. Follow the workaround instructions.

b. Register FIS - Device to Host Command Field Corruption

Problem: If a drive inserts an HOLD/HOLD/Align/Align sequence in a Register FIS from Device to Host FIS with GD31244, a command field corruption can occur. Using NCQ causes delays and a possible hang condition on the SATA link. In non NCQ mode the error condition is processed correctly.

Implication: This sequence inserted in the D-H Register FIS may corrupt the LBA section of the internal copy of the Register FIS.

— In non NCQ mode the LBA section corruption is ignored unless the register FIS has an error and GD31244 handles the error correctly.

— In NCQ mode the LBA section corruption can occur causing delays and a possible hang condition on the SATA link.

Workaround: Do not enable NCQ with GD31244.

Status: No Fix.

c. Set Device Bits FIS - Command Field Corruption in NCQ mode

Problem: If a drive inserts an HOLD/HOLD/Align/Align sequence in a Set Device Bits FIS with GD31244 in NCQ mode, command field corruption can occur causing delays and a possible hang condition on the SATA link.

Implication: This sequence inserted in the Set Device Bits FIS may corrupt the SActive field. Note that the SActive field contains the completion status of commands. This may cause the NCQ commands to be retired improperly.

Workaround: Do not enable NCQ with GD31244.

Status: No Fix.

d. DMA Setup - Command Field Corruption in NCQ mode

Problem: If a drive inserts an HOLD/HOLD/Align/Align sequence in a DMA Setup FIS with GD31244 in NCQ mode, the buffer identifier (TAG) field corruption can occur causing delays with a possible hang condition on the SATA link.

Implication: This sequence may corrupt the TAG field which indicates which of the TAG's (0-31) this DMA transfer is associated with. This may cause the NCQ DMA transfers not to work properly.

Workaround: Do not enable NCQ with GD31244.

Status: No Fix.

e. BIST Activate - Command Field Corruption

Problem: If a drive inserts an HOLD/HOLD/Align/Align sequence in a BIST Activate with GD31244, the two DWord fields may be corrupted.

Implication: This sequence may corrupt the DWord fields which indicate the bit pattern for use in transmitting a known bit pattern on the interface. Do not use BIST with GD31244.

Status: No Fix.

Specification Changes

1. PIO mode is no longer supported.

Due to the erratum #6 Programmed I/O, PIO mode is no longer supported.

2. BIST mode is not longer supported.

Due to the erratum #6 BIST mode is no longer supported.

3. NCQ is not supported.

Due to the erratum #6 NCQ is not supported.

Documentation Changes

1. VCC5REF incorrectly referenced in documentation

Issue: All references to VCC5REF documentation should be renamed as VCCREF.

1. In the 273595-005 Datasheet: on Figure 2 on page 9
2. In the 273595-005 Datasheet: in Table 9 on page 20
3. In the 273595-005 Datasheet: in section 4.3 on page 32

Affected Docs: *Intel® 31244 PCI-X to Serial ATA Controller Datasheet* (273595-005)

2. VCC5REF incorrectly referenced in documentation

Issue: All references to VCC5REF documentation should be renamed as VCCREF.

1. In the 273651-003 Design Guide: On Figure 2 on page 15
2. In the 273651-003 Design Guide: In Table 8 on page 21
3. In the 273651-003 Design Guide: In Table 30 on page 65

Affected Docs: *Intel® 31244 PCI-X to Serial ATA Controller Design Guide* (273651-003)

3. Serial ATA II Native Command Queuing references should be removed.

Issue: Due to the erratum #6 Serial ATA II Native Command Queuing, NCQ is not supported with Intel drivers. All references to NCQ in the GD31244 documentation will be removed this includes:

- Developer's Manual 273603: Section 4.2.5

Affected Docs: *Intel® 31244 PCI-X to Serial ATA Controller Developer's Manual* (273603-006)

4. Reference to support ATAPI CD-ROM and DVD devices should be removed.

Issue: The Developer's Manual 273603: Section 2.4 references connectivity to CD ROMS and DVD ROM's. Intel's GD31244 Windows and Linux drivers do not support a connection to these devices.

Affected Docs: *Intel® 31244 PCI-X to Serial ATA Controller Developer's Manual* (273603-006)

5. PIO mode references should be removed.

Issue: Due to the erratum #6 Programmed I/O, PIO mode is no longer supported. All references to PIO GD31244 documentation includes:

- Developer's Manual 273603: page 48 under Section 4.1 two references on this page.
- Developer's Manual 273603: page 53 under Section 4.2 bullet and Figure 19
- Developer's Manual 273603: page 62 under Section 4.2.4
- Developer's Manual 273603: page 74 under Section 5.3
- Developer's Manual 273603: page 98 under Section 5.7.1
- Developer's Manual 273603: page 166 under Section 5.10.3.1

- Developer's Manual 273603: page 174 under Section 5.10.3.9
- Developer's Manual 273603: page 203under Section 5.10.9.1
- Developer's Manual 273603: page 211 under Section 5.10.9.1

Affected Docs: *Intel® 31244 PCI-X to Serial ATA Controller Developer's Manual* (273603-006)

6. BIST mode references should be removed.

Issue: Due to the erratum #6, BIST mode is no longer supported. All references to BIST in the GD31244 documentation BIST mode includes:

- Developer's Manual 273603: page 48 under Section 4.1.
- Developer's Manual 273603: page 72 under Section 5.2.5.
- Developer's Manual 273603: pages 79-81 under Section 5.5.
- Developer's Manual 273603: page 103 Figure 32.
- Developer's Manual 273603: page 106 Table 35.
- Developer's Manual 273603: page 118 Section 5.10.2.10
- Developer's Manual 273603: pages 187-188, Table 113.
- Developer's Manual 273603: page 221, Table 135.
- Developer's Manual 273603: page 228-237, Section 5.10.12.6.

Affected Docs: *Intel® 31244 PCI-X to Serial ATA Controller Developer's Manual* (273603-006)

7. Incorrect reference to the Serial ATA Specification in the Design Guide

This document references *Serial ATA: High speed Serialized AT Attachment Specification, Revision 1.0e.* This reference should be replaced with *Serial ATA: High speed Serialized AT Attachment Specification, Revision 1.0a.*

- Design Guide 273651: page 13 under Section 2.1.
- Design Guide 273651: page 14 under Section 2.1.
- Design Guide 273651: page 33 under Section 5.4.

Affected Docs: *Intel® 31244 PCI-X to Serial ATA Controller Design Guide* (273651-003)

8. Incorrect reference to the Serial ATA Specification in the Data Sheet

This document references *Serial ATA: High speed Serialized AT Attachment Specification, Revision 1.0e.* This reference should be replaced with *Serial ATA: High speed Serialized AT Attachment Specification, Revision 1.0a.*

- Datasheet 273595: page 1.
- Datasheet 273595: page 7 under Section 1.0.
- Datasheet 273595: page 7 under Section 1.1.
- Datasheet 273595: page 11 under Section 2.3.
- Datasheet 273595: page 34 under Section 4.7.

Affected Docs: *Intel® 31244 PCI-X to Serial ATA Controller Datasheet* (273595-005)

9. Incorrect reference to the Serial ATA Specification in the Data Sheet

This document references *Serial ATA: High speed Serialized AT Attachment Specification, Revision 1.0e.* This reference should be replaced with *Serial ATA: High speed Serialized AT Attachment Specification, Revision 1.0a.*

- Developer's manual 273603: page 22.

Affected Docs: *Intel® 31244 PCI-X to Serial ATA Controller Datasheet* (273603-006)